IN THE CLAIMS

1. (currently amended) A channel reassignment method comprising the steps of:

(a) at a starting point of a reassignment section, making a bridge setting for transmitting a signal on a source channel also onto a destination channel;

(b) interlinking ~~the~~ a pointer operation of a first pointer circuit in said destination channel with a pointer operation of a second pointer circuit in said source channel ~~in all pointer circuits located along said reassignment section~~;

(c) switching the signal from the source channel to the destination channel after performing steps (a) and (b);

(d) clearing the pointer interlinking operation effected in step (b) after performing step (c); and

(e) clearing the bridge setting made in step (a) after performing step (c).

2. (currently amended) A channel reassignment method comprising the steps of:

(a) at a starting point of a reassignment section, making a bridge setting for transmitting a signal on a source channel also onto a destination channel;

(b) interlinking the pointer operation of said destination channel with said source channel in all pointer circuits located along said reassignment section;

(c) switching the signal from the source channel to the destination channel after performing steps (a) and (b);

(d) clearing the pointer interlinking operation effected in step (b) after performing step (c); and

(e) clearing the bridge setting made in step (a) after performing step (c);

~~A method according to claim 1,~~ and further comprising the steps of:

sending a first message to an end point of the reassignment section from the starting point; and

sending a second message from the end point to the starting point in response to the first message, and wherein:

step (b) is performed by being triggered by the first message, and

step (d) is performed by being triggered by the second message.

3. (original) A method according to claim 2, wherein

step (b) is performed at each point located along the reassignment section, step (b) comprising the substeps of:

(i) initiating the pointer interlinking operation upon reception of the first message; and

(ii) transferring the first message after initiating the pointer interlinking operation, and

step (d) is performed at each point located along the reassignment section, step (d) comprising the substeps of:

(i) clearing the pointer interlinking operation upon reception of the second message; and

(ii) transferring the second message after clearing the pointer interlinking

operation.

4. (original) A method according to claim 2, wherein step (c) is performed at each point located along the reassignment section by being triggered by the second message.

5. (original) A method according to claim 1, wherein steps (a), (b), (c), (d), and (e) are performed on both a working channel and a protection channel in parallel fashion.

6. (original) A pointer circuit for performing pointer processing between receiving and transmitting ends of a plurality of channels, the pointer circuit comprising for each channel:

an ES memory temporarily storing payload data of each channel;

a phase comparator generating a stuff request by comparing a write address and read address for the ES memory; and

a pointer determining unit determining a pointer at the transmitting end based on the stuff request, wherein

the pointer circuit further comprises for each channel:

first and second selectors selecting, for a destination channel, a write address and a read address of a source channel as the write address and the read address for the ES memory at the time of channel reassignment, and supplying the selected write address and read address to the ES memory; and

a third selector selecting, for the destination channel, a stuff request of the source channel as the stuff request, and supplying the selected stuff request to the pointer

determining unit.

7. (original) A pointer processing circuit according to claim 6, wherein

the first and second selectors further select, for each of concatenated channels, a write address and a read address of a leading channel of the concatenated channel as the write address and read address, and

selects, for each of concatenated destination channels, the write address and read address of a leading channel of the concatenated destination channel as the write address and read address for the ES memory.